

CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of operating a pixel of an image sensor comprising:

accumulating charge in a photosensor;

transferring said charge from said photosensor to a storage node within said pixel;

transferring said charge from said storage node to a floating diffusion node; and

reading out the charge residing in said floating diffusion node as a pixel output signal.
2. The method of claim 1 further comprising controlling said charge transfer from said photosensor to said storage node with a shutter gate transistor.
3. A method of operating a plurality of pixels of an image sensor comprising:

accumulating a first charge in a first photosensor;

transferring said first charge from said first photosensor to a first storage node within a first pixel;

transferring said first charge from said first storage node to a floating diffusion node;

reading out the first charge from said floating diffusion node as an output signal of said first pixel;

accumulating a second charge in a second photosensor;

transferring said second charge from said second photosensor to a second storage node within a second pixel;

transferring said second charge from said second storage node to said floating diffusion node; and

reading out the second charge from said floating diffusion node as an output signal of said second pixel.

4. The method of claim 3 further comprising the act of sharing said floating diffusion node with a third and fourth pixel, wherein said floating diffusion node is reset, said third pixel accumulates a third charge in a third photosensor, transfers said third charge from said third photosensor to a third storage node within a substrate of said third pixel, transfers said third charge from said third storage node to said floating diffusion node and reads out the third charge from said floating diffusion node as an output signal of said third pixel; and

wherein said floating diffusion node is reset, said fourth pixel accumulates a fourth charge in a fourth photosensor, transfers said fourth charge from said fourth photosensor to a fourth storage node within a substrate of said fourth pixel, transfers said fourth charge from said fourth storage node to said floating diffusion node and reads out the fourth charge from said floating diffusion node as an output signal of said fourth pixel.

5. The method of claim 3, wherein a readout circuit outputs the first and second charges by:

turning on a first transfer gate of the first pixel to transfer the first charge to the floating diffusion node, providing an output signal based on charge at the floating diffusion node with an output transistor and turning

on a row select transistor to output a signal provided by said output transistor; and

turning on a second transfer gate of the second pixel after the readout of said first pixel to transfer the second charge to said floating diffusion node providing an output signal based on charge at the floating diffusion node with an output transistor, and turning on said row select transistor.

6. The method of claim 5, wherein said transferring steps occur on half clock cycles.

7. A method of reading charge from pixels of an image sensor comprising:

turning on a first transfer gate transistor associated with a first pixel to transfer a first charge from a storage node within said first pixel to a floating diffusion node;

providing an output signal of said first pixel with an output transistor coupled to said floating diffusion node;

turning on a row select transistor connected to the output transistor to output the first charge from said floating diffusion node;

while the row select transistor remains on, turning on a second transfer gate transistor associated with a second pixel to transfer a second charge from a storage node within said second pixel to said floating diffusion node; and

providing an output signal of said second output transistor which is output by said row select transistor.

8. The method of claim 7, wherein the transfer of said first and second charges occur on respective half clock cycles.

9. The method of claim 7, wherein said first transfer gate remains on during an integration period.

10. A method of reading charge from pixels of an image sensor comprising:

turning on a first transfer gate transistor associated with a first pixel to transfer a first charge from a storage node within a substrate of said first pixel to a floating diffusion node;

providing an output signal of said first pixel from said first charge stored in said floating diffusion node;

turning on a row select transistor to output said first pixel output signal;

turning on a second transfer gate transistor associated with a second pixel to transfer a second charge from a storage node within said second pixel to said floating diffusion node;

providing an output signal of said second pixel from said second charge stored in said floating diffusion node; and

turning on a row select transistor connected to the floating diffusion node to output said second pixel output signal.

11. A pixel circuit for use in an imaging device, said pixel circuit comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage node connected to said shutter transistor to receive said charge transferred by said shutter transistor;

a transfer gate connected to said storage node to transfer charge from said storage node;

a floating diffusion node connected to said transfer gate to receive said charge from said transfer gate; and

a readout circuit connected to said floating diffusion node to output a signal based on the charge accumulated at the floating diffusion node.

12. A pixel circuit comprising:

a photosensor for accumulating charge;

a first transistor for transferring charge from said photosensor to a first storage node;

a second transistor for transferring charge from said first storage to a second storage node; and

a readout circuit for providing a pixel output signal based on charges transferred to said second storage node.

13. The circuit of claim 12, wherein said readout circuit further comprises:

a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node;

a source-follower transistor connected to said reset transistor for receiving charge from the floating diffusion node; and

a row select transistor connected to said source-follower transistor for outputting a signal produced by said source follower transistor.

14. The circuit of claim 12, wherein said first storage node is formed within said pixel.

15. The circuit of claim 12, wherein a barrier region is coupled to and controlled by said first transistor.

16. The circuit of claim 15, wherein said barrier region is comprised of boron.

17. The circuit of claim 12, wherein said first transistor is an electronic shutter for said pixel circuit.

18. The circuit of claim 12, wherein said first transistor remains on during the integration period.

19. The circuit of claim 12, wherein said pixel circuit is a CMOS pixel.

20. The circuit of claim 12, wherein said pixel circuit comprises five transistors.

21. A pixel circuit comprising:

a plurality of photosensors for accumulating charge;

a plurality of first transistors for transferring charge from a respective one of said photosensors to a respective first storage node;

a plurality of second transistors for transferring charge from said respective first storage node to a respective second storage node; and

a readout circuit for providing a pixel output signal based on charges transferred to said respective second storage node.

22. The circuit of claim 21 wherein said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node prior to receiving charge from a respective one said plurality of transfer gates.

23. The circuit of claim 21, wherein said first storage nodes are formed within said pixel.

24. The circuit of claim 21, wherein a plurality of barrier regions are controlled by a respective one of said first transistors, said barrier region separating said respective photosensor from said respective first storage node.

25. The circuit of claim 21, wherein said first transistors operate as electronic shutters for said pixel circuit.

26. The circuit of claim 21, wherein said first transistors remain on during the integration period.

27. The circuit of claim 24, wherein said barrier regions are comprised of boron.

28. The circuit of claim 21, wherein said pixel circuit is a CMOS pixel.

29. The circuit of claim 21, wherein said pixel circuit is a five transistor pixel.

30. A pixel circuit for use in an imaging device, said pixel circuit comprising:

a plurality of photosensors for generating charge during an integration period;

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor;

a plurality of storage nodes, each node connected to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors;

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage node;

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said storage nodes; and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node.

31. The circuit of claim 30, wherein a plurality of pixel circuits share said floating diffusion node, reset transistor, source follower transistor, and row select transistor.

32. The circuit of claim 30, wherein said pixel circuit is a CMOS pixel.

33. A pixel sensor array comprising:

a plurality of pixels, each pixel comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage node connected to said shutter transistor to receive said charge transferred by said shutter transistor;

a barrier region separating said photosensor from said storage node;

a transfer gate connected to said storage node to transfer charge from said storage node;

a floating diffusion node connected to said transfer gate to receive said charge from said storage node; and

a readout circuit connected to said floating diffusion node to output the charge accumulated at the floating diffusion node.

34. A pixel sensor array comprising:

a plurality of pixels, each pixel comprising:

a photosensor for accumulating charge;

a first transistor for transferring charge from said photosensor to a first storage node;

a second transistor for transferring charge from said first storage to a second storage node; and

a readout circuit for providing a pixel output signal based on charges transferred to said second storage node.

35. The array of claim 34 wherein said readout circuit further comprises a reset transistor connected to said floating diffusion node for resetting the voltage on the floating diffusion node.

36. The array of claim 34, wherein said first storage node is formed within said pixel.

37. The array of claim 34, wherein a barrier region is controlled by said first transistor, said barrier region separating said photosensor from said first storage node.

38. The array of claim 34, wherein said first transistor is an electronic shutter.

39. The array of claim 34, wherein the first transistor remains on during the integration period.

40. The array of claim 37, wherein said barrier region is comprised of boron.

41. The array of claim 34, wherein each pixel is a CMOS pixel.

42. An imaging system pixel comprising:

a processor; and

an imaging device comprising an array of pixels, coupled to said imaging system each pixel comprising:

a photosensor for generating charge during an integration period;

a shutter transistor connected to said photosensor to transfer charge from said photosensor;

a storage node connected to said shutter transistor to receive said charge transferred by said shutter transistor;

a barrier region separating said photosensor from said storage node;

a transfer gate connected to said storage node to transfer charge from said storage node;

a floating diffusion node connected to said transfer gate to receive said charge from said storage node when said transfer gate is activated; and

a readout circuit connected to said floating diffusion node to output the charge accumulated at the floating diffusion node.

43. An imaging system pixel comprising:

a processor; and

an imaging device comprising an array of pixels, coupled to said imaging system each pixel comprising:

a photosensor for accumulating charge;

a first transistor for transferring charge from said photosensor to a first storage node;

a second transistor for transferring charge from said first storage to a second storage node; and

a readout circuit for providing a pixel output signal based on charges transferred to said second storage node.

44. An imaging system comprising:

a processor; and

an imaging device comprising an array of pixels, coupled to said imaging system said array comprising:

a plurality of photosensors for generating charge during an integration period;

a plurality of shutter transistors, each shutter transistor connected to and transferring charge from a respective photosensor;

a plurality of storage nodes, each storage node connected to a respective shutter transistor and storing charge transferred by a respective one of said plurality of photosensors;

a plurality of barrier regions, each barrier region separating a respective photosensor from its respective storage node;

a plurality of transfer gates, each transfer gate connected to and transferring charge from a respective storage node;

a floating diffusion node connected to said plurality of transfer gates for receiving charge from said transfer gates; and

a readout circuit connected to said floating diffusion node to output charge accumulated at the floating diffusion node.

45. An imaging system comprising:

a processor; and

an imaging device comprising an array of pixels, coupled to said imaging system said array comprising:

a plurality of photosensors for accumulating charge;

a plurality of first transistors for transferring charge from a respective one of said photosensors to a respective first storage node;

a plurality of second transistors for transferring charge from said respective first storage node to a respective second storage node; and

a readout circuit for providing a pixel output signal based on charges transferred to said respective second storage node.

46. The system of claim 45, wherein a number of said plurality of photosensors is two photosensors.

47. The system of claim 45, wherein a number of said plurality of photosensors is four photosensors.

48. The system of claim 45, wherein said first transistor is an electronic shutter.

49. The system of claim 45, wherein said first transistor remains on during the integration period.

50. The system of claim 45, wherein a barrier region is controlled by said first transistor, said barrier region separating said photosensor from said first storage node.

51. The system of claim 45, wherein said imaging system is a CMOS imaging system.